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Patent Application

Inventor(s): Nemecek, et al. Group Art Unit: 2123

Filed: 11/14/01 Examiner: Proctor, Jason Scott

Application No.: 10/004,197

Title: IN-CIRCUIT EMULATOR WITH GATEKEEPER BASED HALT CONTROL

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	5,802,290	09/1998	Casselman, Steven M.	709	201	
	B	2002/0156998	10/2002	Casselman, Steven M.	712	227	
	C	2002/0156885	10/2002	Thakkar, Bina Kunal	709	224	
	D	2002/0116168	08/2002	Kim, Mahn Bok	703	28	
	E	6,058,263	05/2000	Voth, David W.	703	25	
	F	6,144,327	11/07/00	Distinti et al.	341	126	8/12/97
	G	5,202,687	04/13/93	Distinti	341	158	6/12/91
	H	5,691,898	11/1997	Rosenberg et al.	700	85	
	I	6,034,538	03/2000	Abramovici, Miron	326	38	
	J	6,816,544	11/2004	Bailey et al.	375	222	
	K	6,967,960	11/2005	Bross et al.	370	410	

→ 6,034,538

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation Yes	Translation No
	L							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	M	Bursky, "FPGA Combines Multiple Interfaces and Logic," Electronic Design, Vol 48 No. 20 pp.74-78 (2 October 2000)
	N	Anonymous, "Warp Nine Engineering-The IEEE 1284 Experts-F/Port Product Sheet," undated web page found at http://www.fapo.com/fport.htm
	O	Anonymous, F/Port: Fast Parallel Port for the PC: Installation Manual: Release 7.1", circa 1997, available for download from http://www.fapa.com/fport.htm
	P	CYPR-CD00182; "IN-SYSTEM CHIP EMULATOR ARCHITECTURE", 10/10/01 09/975,115; Snyder et al.
	Q	CYPR-CD00183; "CAPTURING TEST/EMULATION AND ENABLING REAL-TIME DEBUGGING USING FPGA FOR IN-CIRCUIT EMULATION"; 10/10/01; 09/975,104; Snyder
	R	CYPR-CD00185; "EMULATOR CHIP-BOARD ARCHITECTURE AND INTERFACE"; 10/1/01; 09/975,030; Snyder et al.

	S	CYPR-CD00186; "METHOD FOR BREAKING EXECUTION OF TEST CODE IN A DUT AND EMULATOR CHIP ESSENTIALLY SIMULTANEOUSLY AND HANDLING COMPLEX BREAKPOINT EVENTS"; 10/10/01; 09/975,338; Nemecek et al.
Examiner		Date Considered 2/2/2007

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.